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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/525,598	02/25/2005	Leon Maria Albertus Van De Logt	NL02 0790 US	3615

65913 7590 07/11/2008

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EXAMINER	
TU, CHRISTINE TRINH LE	
ART UNIT	**PAPER NUMBER**
2117	

NOTIFICATION DATE	DELIVERY MODE
07/11/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/525,598	VAN DE LOGT ET AL.	
	Examiner	Art Unit	
	Christine T. Tu	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 February 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *25 February 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Claim Rejections - 35 USC § 112

1. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1:

Throughout the claims, it is not clear what the purpose for reciting "a plurality of outputs" (at line 3). In other words, the plurality of outputs are not interrelated to any other elements among the claim.

Claim 2:

It is not clear how the functional block and the logic gates are interrelated to each others.

Claims 3-7:

These claims are rejected because they depend on claim 1 and contain the same problem of indefiniteness.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

4. Claims 1-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itaya (6,271,700).

Claims 1 and 4:

Itaya discloses the invention substantially as claimed. Itaya shows (figure 1) a semiconductor integrated circuit (10A) having plurality of inputs (SIN, SM, and I1 to In) and plurality of outputs (SOUT, and O1 to Om). The semiconductor integrated circuit (10A) also comprises AND gates (32-35) each having an input connected to the input (*SM) (figure 1, column 3 lines 35-45).

Itaya does not explicitly teach that each AND gate from the plurality of gates having an input coupled to an input from the plurality of inputs. Itaya, however, teaches that each of AND gates (32-35) has a responding input from an output (Q0-Q3) of each of D flip-flops (12-15), wherein the input of the first D flip-flops (12) is coupled to an input (SIN) via a multiplexer (22) (figure 1, column 3 lines 41-45).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Itaya's AND gates each would connected to the input (SIN) directly or indirectly. One having ordinary skill in the art would be motivated to realize so because such connecting each of Itaya's AND gates directly or indirectly to

the input (SIN) would depend on the time and circuitry requirement of the semiconductor integrated circuit.

Claim 2:

Itaya further teaches that a combinational circuit (11) is coupled to plurality inputs (I1 to In) and plurality outputs (O1 to Om) (figure 1).

Claim 3:

Itaya does not explicitly teach the plurality of logic gates comprises XOR gates. Itaya, however, teaches (figure 2) that circuit gates (42 to 45) can be used instead of the AND gates (32 to 35) [of figure 1] (figure 2, column 4 lines 12-18).

It would have been obvious to one having ordinary skill in the art at the time the invention was made to realize that Itaya's circuit gates (42 to 45) would have been XOR gates. One having ordinary skill in the art would be motivated to realize so because Itaya's circuit gates (42 to 45) are not excluded from the inclusive of XOR gates.

Claims 5-7:

Itaya shows plurality of multiplexers (22-25), one (22) of the multiplexers is coupled to an input (SIN) and an input (*SM) and provides an output to the circuit gate (32) via a flip flop (12) (figure 1, column 3 lines 35-64).

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christine T. Tu whose telephone number is (571) 272-3831. The examiner can normally be reached on Mon-Thur. 8:30am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Christine T. Tu/
Primary Examiner
Art Unit 2117

July 1, 2008